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EXAMINER
UNELUS, ERNEST

ART UNIT	PAPER NUMBER
2181	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/707,871	LIU ET AL.	
	Examiner	Art Unit	
	Ernest Unelus	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-22,24-53 and 78-96* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

NJP 7/19/07

6)☒ Claim(s) *1-8,10-22,24-53 and 78-96* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/06/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

RESPONSE TO AMENDMENT

Claim rejections based on prior art

1. Applicant's arguments filed 04/27/2007, with respect to the rejection(s) of claims 1-53, and 78-95 under Bicknell et al. (US pub. 2003/0193776) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US p33ub. 2004/0177218), and Otterness et al. (US pub. 2002/0152355).

2. The instant application having Application No. 10/707,871 has a total of 96 preliminary amended claims pending in the application; there are 4 independent claims and 67 dependent claims, all of which are ready for examination by the examiner.

The applicant cancelled claims 9, 23, and 54-77.

The double patenting rejections are maintained.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

III. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

5. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated July 06, 2007 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

IV. OBJECTIONS TO THE CLAIM

6. **Claims 1-8, 10-22, 24-53, and 78-95** are objected to because of the following informalities: for example, claim 1, line 14 on page 4, discloses, "providing in a said at least…". The letter 'a' should not be place before the word 'said'. This problem should be correct by removing "a".

V. REJECTIONS BASED ON PRIOR ART

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re

Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. **Claims 1-53, and 78-95** is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-62 of copending application No. 11/246,268.

9. Initially, it should be noted that the present application and Application No. 11/246,268, share one common inventor, which is Michael Schnapp. The assignee for both applications is Infortrend Technology, Inc. The examiner also notes that neither the instant application nor U.S application 11/246,268 were the subject of a restriction by the office.

10. Claimed subject matter in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as noted below. *See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993).*

11. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See MPEP § 804.

12. Claim 1 is compared to claims 1 of application 11/246,268 in the following table:

Instant Application	Application 11/246,268
A storage virtualization computer system comprising: a host entity for issuing IO requests; an external storage virtualization controller coupled to said host entity for executing IO operations in response to said IO requests; and at least one physical storage device(PSD), each coupled to the storage virtualization controller through a point-to-point serial-signal interconnect, for providing storage to the storage virtualization computer system through the storage virtualization controller	A patch module comprising: A computer system comprising: a host entity for issuing IO requests; a redundant external storage virtualization controller (SVC) pair for performing IO operations in response to IO requests issued by the host entity comprising a first and a second external SVC coupled to the host entity; and a set of at least one physical storage device (PSD) for providing data storage space to the computer system, with at least one member of said set of at least one PSD comprising a PSD coupled to the said redundant SVC pair through a point-to-point serial signal interconnect for transmission with SAS protocol; wherein when one SVC in the said redundant SVC pair is not on line or goes off line after being on line, the alternate SVC in the said redundant SVC pair will automatically take over the functionality originally performed by the said one SVC in the redundant SVC pair
wherein said storage virtualization controller comprises: a central processing circuitry for performing I0 operations in response to said IO requests of said host entity; at least one i0 device interconnect controller coupled to said central processing circuitry; at least one host-side I0 device interconnect port provided in a said at least one IO	wherein in the redundant SVC pair, each of the SVCs further comprises: a central processing circuitry for performing IO operations in response to IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for

device interconnect controller for coupling to said host entity; and at least one device-side I0 device interconnect port provided in a said at least one I0 device interconnect controller for coupling to a said at least one physical storage device.	coupling to said host entity; and at least one **SAS** device-side IO device interconnect port provided in a said at least one IO device interconnect controller coupled to said at least one PSD through a point-to-point serial-signal interconnect"

This is a provisional double patenting rejection since the conflicting claims have not yet been patented. The double patenting rejection is also applicable to other claims in the instant application and application 11/246,268.

13. **Claim 1** is also provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-49 of copending Application No. 11/246,309.

14. Initially, it should be noted that the present application and Application No. 11/246,309, share one common inventor, which is Michael Schnapp. The assignee for both applications is Infortrend Technology, Inc. The examiner also notes that neither the instant application nor U.S application 11/246,309 were the subject of a restriction by the office.

15. Claimed subject matter in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as noted below. *See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993).*

16. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See MPEP § 804.

17. Claim 1 is compared to claims 1 of application 11/246,309 in the following table:

Instant Application	**Application 11/246,309**
A storage virtualization computer system comprising: a host entity for issuing IO requests; an external storage virtualization controller coupled to said host entity for executing IO operations in response to said IO requests; and at least one physical storage device(PSD), each coupled to the storage virtualization controller through a **point-to-point serial-signa**l interconnect, for providing storage to the storage virtualization computer system through the storage virtualization controller wherein said storage virtualization controller comprises: a central processing circuitry for performing I0 operations in response to said IO requests of said host entity; at least one i0 device interconnect controller coupled to said central processing circuitry; at least one host-side I0 device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and	A storage virtualization computer system comprising: a host entity for issuing IO requests; an external storage virtualization controller coupled to said host entity for executing IO operations in response to said IO requests; and at least one physical storage device (PSD), each coupled to the storage virtualization controller through a **SAS** interconnect, for providing data storage space to the storage virtualization computer system through the storage virtualization controller wherein said external storage virtualization controller comprises: a central processing circuitry (CPC) for performing I0 operations in response to said IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side I0 device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and

at least one device-side I0 device interconnect port provided in a said at least one I0 device interconnect controller for coupling to a said at least one physical storage device.	at least one **SAS** device-side IO device interconnect port provided in a said at least one I0 device interconnect controller for coupling to a said at least one physical storage device.

This is a provisional double patenting rejection since the conflicting claims have not yet been patented. The double patenting rejection is also applicable to other claims in the instant application and application 11/246,309.

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

19. **Claims 1, 21, 78, and 90,** are rejected under 35 U.S.C. 102(e) as being anticipated by Meehan et al. (US pub. 2004/0177218).

20. As per **claims 1, 21, 78, and 90**, Meehan discloses "A storage virtualization computer system **(system 200 of fig. 3)** comprising:

a host entity **(Host 202)** for issuing IO requests;

an external storage virtualization controller **(Primary RAID Controller 205)** coupled to said host entity for executing IO operations in response to said IO requests **(see fig. 3 and paragraph 0014)**; and

at least one physical storage device (PSD) **(Disc drive 1 of fig. 3)**, each coupled to the storage virtualization controller through a point-to-point serial-signal interconnect **(see fig. 3 and paragraph 0029)**, for providing storage to the storage virtualization computer system through the storage virtualization controller **(see paragraph 0029)**,

and wherein in the redundant SVC pair, each of the SVCs further comprises: a central processing circuitry **(microprocessor 406 of fig. 6, as discloses in para. 0028)** for performing IO operations in response to IO requests of said host entity **(see fig. 5 and para. 0028)**;

at least one IO device interconnect controller **(FPGA 409 of fig. 6, as discloses in para. 0028)** coupled to said central processing circuitry **(see fig. 6)**;

at least one host-side IO device interconnect port **(interface connector 410 of fig. 6)** provided in a said at least one IO device interconnect controller for coupling to said host entity **(see para. 0029, which discloses "Data to be written to storage disks 401-404 would move from the host interface 411 (from the host), optionally through a primary RAID Controller (if present), through the Interface connector 410, and into the buffer RAM 407 of RAID Controller 400")**; and

at least one SAS device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupled to said at least one PSD through a point-to-point serial-signal interconnect **(see para. 0029, which discloses "For example, data may be transmitted between the RAID controllers and storage devices by means of an SCA or**

other type Interface Connector 410". See para. 0029 and fig. 6 for SAS transmission and point-to-point serial-signal interconnect).

<u>For all other claims, see the 'Claim Rejections - 35 USC § 103' below</u>

<u>Claim Rejections - 35 USC § 103</u>

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. **<u>Claims 1-16, 20-37, 41-46, 50, 78-83, 86-88, 90-94, and 96</u>**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218).

23. As per **<u>claims 1, 21, 78, and 90</u>**, Bicknell discloses "A storage virtualization computer system **(system 100 of fig. 6)** comprising:

a host entity for issuing IO requests **(Host computer of fig. 6)**;

an external storage virtualization controller **(controller 1)** coupled to said host entity for executing IO operations in response to said IO requests **(see fig. 6 and paragraph 0029)**; and

at least one physical storage device (PSD) **(Disc drive 106.1 of fig. 6)**, each coupled to the storage virtualization controller through a point-to-point serial-signal interconnect **(see fig. 6**

and paragraph 0019), for providing storage to the storage virtualization computer system through the storage virtualization controller **(see paragraph 0027).**

but fails to disclose expressly "transmission with SAS protocol and wherein in the redundant SVC pair, each of the SVCs further comprises: a central processing circuitry for performing IO operations in response to IO requests of said host entity;

at least one IO device interconnect controller coupled to said central processing circuitry;

at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and

at least one SAS device-side IO device interconnect port provided in a said at least one IO device interconnect controller coupled to said at least one PSD through a point-to-point serial-signal interconnect".

Meehan discloses transmission with SAS protocol **(see para. 0029)** and wherein in the redundant SVC pair, each of the SVCs further comprises: a central processing circuitry **(microprocessor 406 of fig. 6, as discloses in para. 0028)** for performing IO operations in response to IO requests of said host entity **(see fig. 5 and para. 0028)**;

at least one IO device interconnect controller **(FPGA 409 of fig. 6, as discloses in para. 0028)** coupled to said central processing circuitry **(see fig. 6)**;

at least one host-side IO device interconnect port **(interface connector 410 of fig. 6)** provided in a said at least one IO device interconnect controller for coupling to said host entity **(see para. 0029, which discloses "Data to be written to storage disks 401-404 would move from the host interface 411 (from the host), optionally through a primary RAID Controller (if present), through the Interface connector 410, and into the buffer RAM 407 of**

RAID Controller 400"); and

at least one SAS device-side IO device interconnect port provided in a said at least one IO device interconnect controller coupled to said at least one PSD through a point-to-point serial-signal interconnect **(see para. 0029, which discloses "For example, data may be transmitted between the RAID controllers and storage devices by means of an SCA or other type Interface Connector 410". See para. 0029 and fig. 6 for SAS transmission and point-to-point serial-signal interconnect).**

Bicknell et al. (US pub. 2003/0193776) and Meehan et al. (US pub. 2004/0177218) are analogous art because they are from the same field of endeavor of redundant array of independent disks (RAID) architectures.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan.

The motivation for doing so would have been because Meehan teaches that **"In addition, a RAID 0 stripe can be written to the storage devices at the same time. This stripe allows for the data to be evenly written to the devices 120 in an attempt to maximize overall system performance" (see paragraph 0006).**

Therefore, it would have been obvious to combine Meehan et al. (US pub. 2004/0177218) with Bicknell et al. (US pub. 2003/0193776) for the benefit of creating the computer system to obtain the invention as specified in claims 1, 21, 78, and 90.

24. As per **claims 2, 22, 79, and 91**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein said point-to-point serial-signal interconnect is a Serial ATA IO device interconnect **(see fig.6 and paragraph 0019).**

25. As per **claims 3, 26, 86, and 92**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein a said at least one PSD comprises a SATA PSD **(see paragraph 0019).**

26. As per **claims 4, 30, 87, and 93**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein a said at least one PSD comprises a PATA PSD and a serial-to-parallel converter **(data interface 144 of fig. 6)** is provided between said device-side IO device interconnect controller and said PATA PSD **(see paragraph 0030).**

27. As per **claims 5 and 31**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses comprising a detachable canister attached to said storage virtualization controller for containing a said at least one PSD therein **(see paragraph 0019, which discloses "Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100").**

28. As per **claims 6 and 32**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein a said at least one PSD can be detached from said storage virtualization controller when said storage virtualization controller is on-line **(see paragraph 0019, which discloses "Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100")**.

29. As per **claims 7 and 33**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein a said at least one PSD can be attached to said storage virtualization controller when said storage virtualization controller is on-line **(see paragraph 0030).**

30. As per **claims 8 and 28**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein said storage virtualization controller is configured to define at least one logical media unit consisting of sections of at least one said PSD **(paragraph 0007 of the applicant's specification discloses "*A RAID controller combines sections on one or multiple physical direct access storage devices (DASDs), the combination of which is determined by the nature of a particular RAID level, to form logical media units*"; similarly, Bicknell discloses, in fig. 6, a RAID controller combines sections on one or multiple physical direct access storage devices)**.

31. As per **claims 10 and 24**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Meehan discloses wherein a said host-side IO device interconnect port and a said device-side IO device interconnect port are provided in the same IO device interconnect controller **(see para. 0029 and fig. 6).**

32. As per **claims 12 and 27**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein said storage virtualization controller comprises a plurality of host-side IO device interconnect ports each for coupling to a host-side IO device interconnect **(see fig. 6 and paragraph 0026).**

33. As per **claims 13 and 29**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein said storage virtualization controller is configured to present redundantly a logical media unit on at least two of said plurality of host-side IO device interconnect ports **(see paragraph 0019).**

34. As per **claims 14 and 35**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at least one said host-side IO device interconnect port is Fibre Channel supporting point-to-point connectivity in target mode **(see paragraph 0030 and fig. 6).**

35. As per **claims 15 and 36**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at

least one said host-side IO device interconnect port is Fibre Channel supporting private loop connectivity in target mode **(see paragraph 0030 and fig. 6)**.

36. As per **claims 16 and 37**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at least one said host-side IO device interconnect port is Fibre Channel supporting public loop connectivity in target mode **(see paragraph 0032 and fig. 6)**.

37. As per **claims 20 and 41**, the combination of Bicknell and Meehan discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at least one said host-side IO device interconnect port is Serial ATA operating in target mode **(see paragraph 0019).**

38. As per **claims 34 and 96**, the combination of Bicknell and Meehan discloses "The virtualization subsystem of claim 21" **[See rejection to claim 21 above]** Bicknell discloses wherein said storage virtualization controller further comprises at least one multiple-device device-side expansion port **(Midplane Card ports 209 of fig. 6)** for accommodating an additional set of at least one PSD **(see fig. 6)**.

39. As per **claims 42 and 80**, the combination of Bicknell and Meehan discloses "The virtualization subsystem of claim 21" **[See rejection to claim 21 above]** Bicknell discloses comprising an enclosure management services mechanism **[(MUX 208 of fig. 8), in regards to**

an "enclosure management service", the applicant discloses "*In this embodiment, an enclosure management service (EMS) circuitry 360 is attached to the CPC 240 for managing and monitoring at least one of the following devices belonging to the storage virtualization subsystem 20: power supplies, fans, temperature sensors, voltages, uninterruptible power supplies, batteries, LEDs, audible alarms, PSD canister locks, door locks*". Similarly, Bicknell discloses "The multiplexing electronics selectively opens and closes the first and second data communication paths in response to at least one control signal (such as 218 or 220) "see paragraph 0037. The electronics connection, as discloses, is power supplies].

40. As per **claim 43**, the combination of Bicknell and Meehan discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism manages and monitors at least one of the following devices belonging to the storage virtualization subsystem: power supplies, fans, temperature sensors, voltages, uninterruptible power supplies, batteries, LEDs, audible alarms, PSD canister locks, door locks **(see paragraph 0031).**

41. As per **claim 44**, the combination of Bicknell and Meehan discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism is configured to support direct-connect EMS configuration **(see fig. 8)**.

42. As per **claim 45**, the combination of Bicknell and Meehan discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism is configured to support device-forwarded EMS configuration **(see fig. 8)**.

43. As per **claims 46, 81, 82, and 83**, the combination of Bicknell and Meehan discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism is configured to support direct-connect EMS configuration and device-forwarded EMS configuration **(see fig. 8)**.

44. As per **claim 50**, the combination of Bicknell and Meehan discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said EMS mechanism further comprises status-monitoring circuitry to communicate with said storage virtualization controller **(see paragraph 0031).**

45. As per **claims 88 and 94**, the combination of Bicknell and Meehan discloses "The method of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein the step of performing said at least one IO operation comprises issuing at least one device-side IO request to said device-side IO device interconnect controller and reformatting said device-side IO request and accompanying IO data into at least one data packet for transmission **(see paragraph 0030).**

46. **Claims 11 and 25,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) as applied to claim 1 above, and further in view of Otterness et al. (US pub. 2002/0152355).

47. As per **claims 11 and 25,** the combination of Biknell and Meehan discloses "The storage virtualization computer system of ćlaim 1," **[See rejection to claim 1 above]** , but fails to disclose expressly wherein said at least one IO device interconnect controller comprises a plurality of IO device interconnect controller; wherein said host-side I0 device interconnect port and said device-side I0 device interconnect port are provided in different said IO device interconnect controllers.

Otterness discloses "wherein said at least one IO device interconnect controller comprises a plurality of IO device interconnect controller; wherein said host-side I0 device interconnect port and said device-side I0 device interconnect port are provided in different said IO device interconnect controllers" **(see fig. 4, which discloses a controller such as a RAID controller 199 having a processor 216 such as the 'central processing circuit' as claimed. Fig. 4 also discloses multiple processor/memory controllers 204 and 206 connected to the processor 216. Multiple processor/memory controllers 204 and 206 are shown to have their own device port and host port. See para. 0048 for more detail).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Otterness et al. (US pub. 2002/0152355) are analogous art because they are from the same field of endeavor of redundant array of independent disks (RAID) architectures.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, and device interconnection topologies, and methods for communicating data or other information between such devices; more particularly to inter- and intra-device connection and communication topologies and methods for such communication; and most particularly to RAID storage system controllers that increase available storage device interconnect channel capacity by routing controller-to-controller messages to a communication channel separate from the communication channel normally used to communicate the RAID data as taught by Otterness.

The motivation for doing so would have been because Otterness teaches that " **Embodiments of the NorthBay.TM. provides support services for a RAID controller. Among other things, the NorthBay ASIC implements a fast special-purpose-processor that computes the parity values used in the RAID system. The data for which the NorthBay ASIC is to handle memory operations and compute parity is specified by the RAID controller's CPU in response to host disk transactions" (see paragraph 0018).**

Therefore, it would have been obvious to combine Otterness et al. (US pub. 2002/0152355) and Meehan et al. (US pub. 2004/0177218) with Bicknell et al. (US pub. 2003/0193776) for the benefit of creating the storage virtualization computer system to obtain the invention as specified in claims 11 and 25.

48. **Claims 17, 19, 38, 40, 47, 48, 84, and 85**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) as applied to claim 1 above, and further in view of Rabinovitz et al. (US pat. 6,483,107).

49. As per **claims 17, 19, 38, and 40**, Bicknell and Meehan discloses "The computer system of claim 1," **[See rejection to claim 23 above]**, including at least one said host-side IO device interconnect port is parallel/serial operating in target mode **(see paragraph 0030)**, but fails to disclose expressly a SCSI.

Rabinovitz discloses a SCSI in a storage virtualization subsystem **(col. 16, line 49).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Rabinovitz et al. (US pat. 6,483,107) are analogous art because they are from the same field of endeavor of peripheral storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, and a canister and a casing of a computer peripheral enclosure as taught by Rabinovitz.

The motivation for doing so would have been because Rabinovitz teaches that a SCSI allows more connecting storage devices **(see col. 16, lines 43-54).**

Therefore, it would have been obvious to combine Rabinovitz et al. (US pat. 6,483,107) with Bicknell et al. (US pub. 2003/0193776) and Meehan et al. (US pub. 2004/0177218) for the benefit of creating the storage virtualization subsystem to obtain the invention as specified in claims 17 and 38.

50. As per **claims 47 and 84**, Bicknell and Meehan discloses "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]**, including the enclosure management services mechanism **(MUX 208 of fig. 8)**, but fails to disclose expressly wherein said enclosure management services mechanism is configured to support SES enclosure management services protocol.

Rabinovitz discloses a SES in a storage virtualization subsystem **(col. 17, line 23).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Rabinovitz et al. (US pat. 6,483,107) are analogous art because they are from the same field of endeavor of peripheral storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, and a canister and a casing of a computer peripheral enclosure as taught by Rabinovitz.

The motivation for doing so would have been because Rabinovitz teaches that a SES allow a user to monitor the enclosure from a remote location **(see col. 17, lines 29-31).**

Therefore, it would have been obvious to combine Rabinovitz et al. (US pat. 6,483,107) with Bicknell et al. (US pub. 2003/0193776) and Meehan et al. (US pub. 2004/0177218) for the benefit of creating the storage virtualizàtion subsystem to obtain the invention as specified in claims 47 and 84.

51. As per **claims 48 and 85**, the combination of Bicknell, and Meehan, and Rabinovitz discloses "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]** Bicknell discloses the enclosure management services mechanism, and Rabinivitz further discloses the SAF-TE, **(see col. 17, line 29).**

52. **Claims 18, 39, 49, 51, 52, and 53**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) as applied to claim 1 above, and further in view of Colton (US pub. 2005/0089027).

53. As per **claims 18 and 39**, Bicknell and Meehan discloses "The computer system of claim 1," **[See rejection to claim 1 above]**, including at least one said host-side IO device interconnect port **(see fig. 6)**, but fails to disclose expressly wherein at least one said host-side IO device interconnect port is ethernet supporting the iSCSI protocol operating in target mode.

Colton discloses ethernet supporting the iSCSI protocol operating in target mode **(see fig. 11 and paragraph 1487, which discloses internet SCSI in an Ethernet network).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Colton (US pub. 2005/0089027) are analogous art because they are from the same field of endeavor of data transfer.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, and a system and method for transferring data optically via an intelligent optical switching network as taught by Colton.

The motivation for doing so would have been because Colton teaches that **"The Sun server(s) running Oracle should have a minimum of 2 high-speed SCSI disk drives to ensure adequate performance" (see paragraph 1487).**

Therefore, it would have been obvious to combine Colton (US pub. 2005/0089027) with Bicknell et al. (US pub. 2003/0193776) and Meehan et al. (US pub. 2004/0177218) for the benefit of creating the computer system to obtain the invention as specified in claims 18 and 39.

54. As per **claims 49, 51, and 53**, the combination of Bicknell, Meehan, and Colon discloses "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]** Bicknell discloses the enclosure management services mechanism and a storage virtualization controller **(see fig. 8)**, and Colon further discloses 12C latches, **(see fig. 11).**

55. As per **claim 52**, the combination of Bicknell, Meehan, and Colon discloses "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]** Bicknell discloses the enclosure management services mechanism as a micro-computer **(see fig. 8)**, and Colon further discloses a CPU for running a program, **(see paragraph 0810 and fig. 11).**

56. **Claims 89 and 95**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) as applied to claim 1 above, and further in view of Johnson et al. (US pub. 2003/0033477).

57. As per **claims 89 and 95**, Bicknell and Meehan discloses "The method of claim 88," **[See rejection to claim 88 above]**, but fails to disclose expressly "wherein said data packet comprises a start segment at the beginning indicating the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual IO information to transmit through the device-side IO device interconnect, and á check data segment containing check codes derived from said payload data for checking the correctness of said payload data after transmission"

Johnson discloses "wherein said data packet comprises a start segment at the beginning indicating the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual IO information to transmit through the device-side IO device interconnect, and a check data segment containing check codes derived from said payload data for checking the correctness of said payload data after transmission" **(see paragraph 0025).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218) and Johnson et al. (US pub. 2003/0033477) are analogous art because they are from the same field of endeavor of redundant array of independent disks (RAID) data storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, and a system generally relates to the field of information handling systems including computer systems and related devices using redundant array of independent disks (RAID) data storage systems and, more particularly, to a system and method for RAID striped data transfer
as taught by Johnson.

The motivation for doing so would have been because Johnson teaches that **" In general, each SGL entry contains an address and a length and may contain flags, such as Size of Address (i.e., 32-bit or 64-bit), End of List Reached, direction of data transfer, and the like" (see paragraph 0024).**

Therefore, it would have been obvious to combine Johnson et al. (US pub. 2003/0033477) with Bicknell et al. (US pub. 2003/0193776) and Meehan et al. (US pub. 2004/0177218) for the benefit of creating the computer system to obtain the invention as specified in claims 89 and 95.

VI. RELEVANT ART CITED BY THE EXAMINER

58. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

59. The following reference teaches a storage virtualization computer system.

U.S. PATENT NUMBER

US 5,987,566

VII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

60. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

61. Per the instant office action, claims 1-8, 10-22, 24-53, and 78-96 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

62. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

63. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PMR system, see her//pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

July 11, 2007

Ernest Unelus
Patent Examiner
Art Unit 2181

/Ernest Unelus/
7/19/2007